REMARKS

These remarks follow the order of the paragraphs of the office action. Relevant portions of the office action are shown indented and italicized. Claims 1-21 remain in the application. Claims 1, 2, 4, 7, 9, 10, 18, 19, 20 and 21 are amended herewith.

Applicants' representative wishes to express gratitude for the Examiner's advice to bring this application to allowance.

DETAILED ACTION

Response to Arguments

1. Per the drawings, Fig. 2, element 270 should be labeled "170" based on the specification, page 6, line 22. Fig. 4 also has a conflicting label "170". In the Fig. 3. "USER SPACE' does not have a corresponding numeric label (pg. 8, third paragraph indicates it should he referenced as "90") Fig. 5, the PLB is no numeric labeled (pg. 15, third paragraph indicates (should be referenced as "390").

In response, the applicants respectfully state that the Figures 2, 3 4 and 5 are amended and a complete set of drawings is provided herewith.

The specification is amended to reflect that the 'i chache' is labeled 175.

2. The objection to the specification has been withdrawn.

3. Applicant's arguments filed 11/17/2006, with respect to the 35 U.S.C. §112 rejections have been fully considered and are persuasive. The 35 U.S.C. § 112 rejections of claims 1-20 has been withdrawn.

In response, the applicants respectfully state their appreciation for the withdrawal of the objections under 35 U.S.C. § 112.

4. Applicant's arguments filed 11/17/2006 with respect to the 33 U.S.C. §101 rejections of claims 1-8 have been fully considered but they are not persuasive. The limitations for

claim 1 can be purely functional descriptive material, per se, and do not require associated hardware. This is nonstatutory per MPEP 2106.01

In response, the applicants respectfully state that claim 1 is amended to specifically include hardware. This overcomes the rejection under 33 U.S.C. §101, and claim becomes allowable.

The arguments for 35 U.S.C. §101 rejections of claims 17-19 have been fully considered and are persuasive. The corresponding rejections are hereby withdrawn.

5. It is noted that applicant will file a terminal disclaimer to vacate the double patenting rejection. The double patenting rejection will be maintained herein, until the terminal disclaimer is filed and approved.

In response, the applicants respectfully state that applicants plan to file a terminal disclaimer once allowable subject matter is identified.

6. Applicant's arguments filed 11/17/2006 with respect to the prior art have been fully considered but they are not persuasive. Examiner rebuttal is detailed below.

Applicant argues against the equivalence of "multistream data packet transfer" cited by the prior art to Yee at a1 (Yee) and the claim language "controlling data flow" between processing systems (pg. 16 lines 11-13 of Remarks). Examiner does not agree since "controlling data flow" simply refers to handling how a data is transmitted from one destination to another Yee anticipates this, where data streams (by definition being data flows) are controlled by an interface controller (Fig 1, element 116) directing the data streams from a memory (Fig. 1) element 106, to processors (Fig. 1, elements 110 or 112). Column 3, lines 40-50 and Column 4, lines 20-45 further disclose the user of descriptors which assist the interface controller in knowing where the next set of data is, the size of the data, the size of data left to transfer, etc.

Applicant next argues that "descriptor logic" is not used in the same sense as the claims and as described in the specification (pg. 17, lines 22-27 of Remarks). Examiner does not agree.

First, the claims are silent as to the details of the structure of the descriptor logic. Any hardware/software structural configuration can read on the "descriptor logic". Turning to the specification, there is little more detail to descriptor logic, only that it "generates and modify the descriptors according to control measures to be taken" (pg. 26, lines 6-13). Yee meets the above by showing various descriptor logic in Fig. 3, portions of the descriptor logic dealing with creation and use (Fig. 3, element 150). Applicant next argues that Yee uses similar wording as the claims, however Yee is intended for a different context (pg. 18, Lines 19-23) and that "descriptor logic" is used in a different sense in Yee. Examiner does not agree, the metes and bounds of the current set of claim language encompasses Yee in scope. Examiner recommends additional claim language to limit the context of the claims to that of what Applicant intends.

Applicant next argues for claims 3 and 13 that Yee is not concerned with descriptor logic in the same sense as the instant application. Examiner reapplies his previous rebuttal above, on this matter.

In response, the applicants respectfully state that they stand by their previous arguments.

However, claims are amended herein to bring the application to allowance quickly.

7. Applicant's arguments, filed 11/17/2006, with respect to the 35 U.S.C. 103(a) rejection of claims 4-6, 13 and 14 have been fully considered and are persuasive. The 35 U.S.C. 103(a) of claims 4-6, 13 and 14 has been withdrawn.

In response, the applicants respectfully state their appreciation for the withdrawal of the objections under 35 U.S.C. 103(a).

Drawings

8. The drawings are objected to because Fig. 2, element 270 should be labeled "170" based on the specification, page 6, line 22. Fig. 4 also has a conflicting label "170". In the Fig. 3, "USER SPACE" does not have a corresponding numeric label (pg. 8, third paragraph indicates it should be referenced as "90"). Fig. 5, the PLB is no numeric labeled (pg. 15, third paragraph indicates it should be referenced as "390"). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

In response, the applicants respectfully state that the Figures 2, 3 4 and 5 are amended and a complete set of drawings is provided herewith.

Claim Objections

9. Claim 18 objected to because of the following informalities: the claims should be clarified as follows: in line 13, after the terms "data processing system", insert ", the

data processing system". This clarifies the antecedent basis related to the ensuing term "comprising".
Appropriate correction is required.

In response, the applicants respectfully state that claim 18 is amended to overcome the objection.

Claim Rejections -35 USC § 101

10. 35 U.S.C. 101 reads as follows: Whoever invents or discovers any new and useful process, machine, composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claims 1-8 are rejected under 35 U.S.C. 101 because the claims are not limited to tangible embodiments. Claim 1 purport to be an apparatus, however there are no hardware limitations describing the apparatus. The added limitation to computer readable medium can also not be hardware based. A descriptor logic, pointer descriptor and descriptor table are used by the apparatus but not part of the claim apparatus. They can purely be functional descriptive material, per se, and do not require associated hardware according to claim 1. Claims 2-8 are rejected based on being dependent on a rejected base claim.

In response, the applicants respectfully state that claim 1 is amended to specifically state that it is comprised of hardware.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In c Berg, 140 F.3d 1428,46 USPQ2d 1226 (Fed. Cir. 1998); In se Goodman, 11 F.3d 1046,29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In se Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).
A timely filed terminal disclaimer in compliance with 37 CFR 3.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be

commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must frilly comply with 37 CFR 3.73(b).

13. Claims 1-21 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-20 of copending Application No. 10/619960 based on reasons stated in the previous Office Action. This is a provisional obviousness-type double patenting rejection.

In response, the applicants respectfully state that applicants plan to file a terminal disclaimer once allowable subject matter is identified.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless- (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this sub-subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 1,2,7-11 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. No. 6,466,581 to Yee et al. (Yee).

In response, the applicant respectfully states that exception is taken with the equivalencies of Claims 1,2,7-11 and 15-20 and Yee. The claims are apparently not anticipated by Yee. The present invention, claimed in Claims 1,2,7-11 and 15-20, provides:

"Apparatus, methods and systems for controlling data flow between data processing systems. In an example embodiment, the apparatus includes descriptor logic for generating a plurality of descriptors including a frame descriptor defining a data packet to be communicated between a location in the memory and a data processing system, and a pointer descriptor identifying the location in the memory. The apparatus also includes a

descriptor table for storing descriptors generated by the descriptor logic for access by the data processing systems.

Whereas, the cited art to Yee, US Patent 6,466,581, filed: August 3, 1998, is entitled: "Multistream data packet transfer apparatus and method". The abstract reads : "A multistream data packet transfer apparatus and method receives data for at least one stream of multistream data from multiple fragments of memory, over a bus from a first processor. The first processor stores multistream data in the fragmented memory. An interface controller, such as any suitable logic and /or software, evaluates the received data to determine which received data is usable data for a second processor. A data packer removes unusable data and packs the usable data in fixed sized units to form a data packet for the second processor. The data packer packs data received from different fragments of memory as a single packet for use by a DSP requesting the information ".

Thus, Yee is concerned with multistream data packet transfer not with controlling data flow between data processing systems. Thus Claims 1,2,7-11 and 15-20 are not anticipated by Yee and should be allowable over Yee. However, claim 1 and all other independent claims are amended to bring the application to allowance quickly.

16. Per claim 1. Yee discloses an apparatus (Fig. 1 is a multistream data packet transfer apparatus; Column 3 lines 20-35 describe the apparatus in .short) comprising: descriptor logic (Fig 3 shows various logic elements that directly deal with creation and use; Fig. 3, element 150, for instance contains descriptors describing location of descriptor table and size of data needed: Fig. 3 element 106 contains descriptor table containing various descriptor entries) on a computer readable medium (Fig. 3, element 122), said apparatus for controlling flow of data (descriptors control how "data streams" are utilized in multimedia processing in the apparatus of Fig. 1; The "data streams" are by definition "flows of data" used in real-time multimedia applications. The descriptors in Yee control how the data streams are processed; Fig 4 is an illustration how data streams are controlled via descriptors) between first and second data processing systems (Fig. 1, descriptor logic elements 100 and 106 contra/flow of data between host system CPU, element 104 and DSP's. elements 110 and 112; the host CPU is representative of the first data processing system and the DSPs are representative of the second data processing system), via a memory (Figs. 1 and 3, element 106 show the descriptors that control the flow of data being stored in system memory), said descriptor logic generating, a plurality of descriptors (Fig. 3, elements 150 and 107; Column 7,

lines 1+ disclose generating descriptors that tracks up to 32 active data streams) including a frame descriptor defining a data packet to be communicated between a location in the memory and the second data processing system (Fig. 3, elements 150; Column 3, lines 40-50 and Column 7, lines 33-40 disclose a descriptor that defines the size information of the data stream, the data stream being associated with a data packet, "For each stream, one register in the groups contains...the 'size of descriptor table "; the descriptor table is in the memory, Fig. 3, element 106 and contains detailed information about each stream and how the DSPs should handle the stream, see Column 1, lines 43-51. Note, nowhere in this limitation describes in any detail whatsoever what it means to define a data packet, i.e., it could be a partial definition or a full definition of all the details of a data packet or it can be simple a pointer to another location where the data packet is defined, etc.), a pointer descriptor identifying the location in memory (Fig. 3, elements 150; Column 3, lines 40-50, "...descriptor table address location"); and a descriptor table for storing on a computer readable medium, the descriptors generated by the descriptor logic for access by the first and second data processing systems (Fig. 3, element 107).

In response, the applicants respectfully state that although applicants maintain their opinion regarding the cited art, claim 1 is amended to bring the application to allowance. Claim 1 as amended includes limitations of: wherein said apparatus employs Logical Communication Port architecture; wherein said Logical Communication Port architecture comprises LCP Clients, an LCP Manager resident in the kernel space, and at least one LCP Context resident in an adapter; and wherein an LCP client can be located in one of user application space and the kernel. Thus claim 1 and all claims that depend on claim 1 are allowable.

17. Per claims 9,10,17-20, claim 1 is substantially similar to claims 9,10,17-20 and therefore the rejection is applied accordingly. Yee discloses an associated method with the apparatus of claim 1 (Figs. 4 and 6), as well as associated computer program product (Fig. 1), program storage device (Fig 3, element 122 and 106) and article of manufacture (Fig 1). Specifically for claim 9, Fig. 1 is construed to be the data processor unit of the preamble, the data communication interface is the bus between host CPU and DSP units. The PCI bus (Fig. 1, element 108) can communicate with multiple device that is attached to it, being construed here as the data communications network of the multiple devices.

In response, the applicants respectfully state that although applicants maintain their opinion regarding the cited art, Claims 9, 10, 18, 19 and 20 is amended to bring the application to allowance. Claims 9, 10, 18, 19 and 20 as amended include limitations of: to employ Logical Communication Port architecture; wherein said Logical Communication Port architecture

comprises LCP Clients, an LCP Manager resident in the kernel space, and at least one LCP Context resident in an adapter; and wherein an LCP client can be located in one of user application space and the kernel. Thus Claims 9, 10, 18, 19 and 20 and all claims that depend on Claims 9, 10, 18, 19 and 20 are allowable.

18. Per claims 2, 7,11 and 15, Yee discloses claims 1 and 10, Yee further discloses using a Logical Communications Port architecture (LCP is very generally defined on page 8, lines 18-26 as "...a framework for the interface between local consumers running on the host computer and adapter". It further goes onto using open-ended language as to suggest what LCPs could have; Yee discloses interfacing between a host and secondary DSP systems. e.g., the consumers and producers, via an controller adapter, element 100, meeting this general definition of LCP), and the descriptor table is stored in the first data processing system (Fig. 3, element 106 is system memory, by definition being the host CPU memory as shown in Fig. 1). The first data processing system comprises a host computer system (Fig. 1, element 104, host CPU).

In response, the applicants respectfully state that claims 2, and 7 are amended to be commensurate with claim 1. Claims 2, 7, 11 and 15 are allowable each for itself as stated previously and because each depends on an allowable claim.

19. Per claims 8 and 16, Yee discloses claims 1 and 10, Yee further discloses the second data processing system (Fig. 1, elements 110 and 112.) comprising a data communication interface (Fig. 1, buses 130 and 132) for communicating data between host computer (Fig. 1, element 104) and data communications network (Fig. 1, element 108.).

In response, the applicants respectfully state that claims 8, and 16 are allowable each for itself as stated previously, and because each depends on an allowable claim.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentabilty shall not be negatived by the manner in which the invention was made.

21. The factual inquiries set faith in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966). that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

22. This application currently names joint inventors. In considering patentability of the claims under 33 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CPR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

23. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yee.

Yee discloses claims 1 and 10 of which claims 3 and 12 depend. Yee further discloses descriptor tables being accessible by the second processing system (Fig. 4, descriptors let DSP access data streams for processing). Yee does not disclose expressly the descriptor table being stored in the second processing system.
At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the descriptor tables in the second processing system, where the DSP units (Fig. 3, elements 110 and 112) are located.
The suggestion/motivation for doing so would have been a matter of design choice. Yee has the host processor generate the descriptor tables (Fig. 4, element 200.), so the host system memory (Fig. 3, element 106) would logically be used to store the descriptor tables, which Yee does (Fig 3. element 107). However, the tradeoff here is the increased latency subjected to the DSP units in reading from the descriptor tables, having to traverse multiple interfaces (Fig. 3, PCI bus, at minimum. must be arbitrated for to get access to Descriptor Tables.). If the host processor stored the descriptor tables in a memory directly connected to DSP units, the latency to access the descriptor tables by the DSP units would be significantly reduced, with the tradeoff here being host write of descriptor tables being slower. Therefore, it would have been obvious to implement the descriptor tables on the second data processing system for faster access by the DSP units.

In response, the applicants respectfully state that claims 3, and 12 are allowable each for itself as stated previously, and because each depends on an allowable claim.

It is anticipated that this amendment brings claims 1-21 to allowance. If any questions remain, please contact the undersigned representative.

Please charge any fee necessary to enter this paper to deposit account 50-0510.

Respectfully submitted,

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